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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,414	09/30/2003	Juha-Veikko Voutilainen	KOLS.060PA	6185

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EXAMINER
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VUONG, QUOCHIEN B

ART UNIT	PAPER NUMBER
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2618

DATE MAILED: 06/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/675,414

Applicant(s)

VOUTILAINEN ET AL.

Examiner

Quochien B. Vuong

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 September 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Information Disclosure Statement***

1. The information disclosure statement (IDS) submitted on 01/05/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).
4. Claims 1-10, 12-23, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Telewski (US 6,021,315) in view of Thatcher et al. (US 5,968,191).

Regarding claims 1, 14 and 26, Telewski discloses a method and an arrangement for testing an electric circuit of a wireless device of a telecommunications system (column 1, lines 23-29). Telewski does not disclose the method including: supplying current to at least one current path of a network of electric components, the network being characterized with a predefined network configuration; measuring effective values of node voltages in at least two nodes of the at least one current path, a node representing an equipotential point of adjacent electric components; and deriving a characterizing value of at least one electric component of the network by using the effective value of the current, the effective values of the node voltages, and the predefined network configuration. However, Thatcher et al. (figure 2) disclose the method and arrangement for testing an electric circuit comprising supplying current to at least one current path of a network of electric components, the network being characterized with a predefined network configuration; measuring effective values of node voltages in at least two nodes of the at least one current path, a node representing an equipotential point of adjacent electric components; and deriving a characterizing value of at least one electric component of the network by using the effective value of the current, the effective values of the node voltages, and the predefined network configuration (column 3, lines 4-46). Therefore, it would have been obvious to adapt the teaching of Thatcher et al. to the method and arrangement of Telewski in order to test each component of the electric circuit as desired to ensure the quality or design.

Regarding claims 2 and 15, Telewski and Thatcher et al. disclose the method and arrangement of claims 1 and 14 above, respectively. In addition, Thatcher et al

disclose wherein the characterizing value of the at least one electric component depends on the frequency of current (column 3, lines 35-46).

Regarding claims 3 and 16, Telewski and Thatcher et al. disclose the method and arrangement of claims 1 and 14 above, respectively. In addition, Telewski and Thatcher et al. if not inherent would be obvious to disclose wherein the step of deriving includes calculating the characterizing value with a closed-form mathematical expression formed according to the predefined network configuration in order to calculate the characterizing value (column 3, lines 35-46).

Regarding claims 4 and 17, Telewski and Thatcher et al. disclose the method and arrangement of claims 1 and 14 above, respectively. In addition, Thatcher et al further disclose deriving the characterizing value by using the frequency associated with current (column 3, lines 35-46).

Regarding claims 5-6 and 18-19, Telewski and Thatcher et al. disclose the method and arrangement of claims 1 and 14 above, respectively. In addition, Thatcher et al further disclose deriving the characterizing value by using a priori characterizing value; measuring effective values of node voltages of an electric component which has a known characterizing value; and deriving the value of current by using the effective values of the node voltages of the electric component which has the known characterizing value, and the known characterizing value (column 1, line 66 – column 2, line 3; and column 3, lines 4-46).

Regarding claims 7 and 20, Telewski and Thatcher et al. disclose the method and arrangement of claims 1 and 14 above, respectively. In addition, Thatcher et al

further disclose accessing the network with a standardized boundary scan test structure in order to measure the effective values of the node voltages (column 1, lines 60-65).

Regarding claim 8, Telewski and Thatcher et al. disclose the method and arrangement of claim 1 above. In addition, Thatcher et al further disclose accessing the network with a standardized boundary scan test structure in order to supply the current to the at least one current path (column 1, lines 60-65).

Regarding claims 9 and 21, Telewski and Thatcher et al. disclose the method and arrangement of claims 7 and 20 above, respectively. In addition, Thatcher et al wherein at least a portion of the network and at least a portion of the test structure are placed on a one and the same integrated circuit (see figure 2).

Regarding claim 10, Telewski and Thatcher et al. disclose the method and arrangement of claim 8 above. In addition, Thatcher et al wherein at least a portion of the network and at least a portion of the test structure are placed on a one and the same integrated circuit (see figure 2).

Regarding claims 11 and 24, Telewski and Thatcher et al. disclose the method and arrangement of claims 1 and 14 above, respectively. a delta configuration.

Regarding claims 12 and 25, Telewski and Thatcher et al. disclose the method and arrangement of claims 1 and 14 above, respectively. In addition, Thatcher et al wherein the characterizing value of an electric component represents a value of an electric quantity selected from a group including: resistance, capacitance, inductance, conductance, impedance (column 1, line 66 – column 2, line 3).

Regarding claims 13, Telewski and Thatcher et al. disclose the method of claim 1 above. In addition, Thatcher et al further including supplying current to a plurality current paths; and measuring effective values of the values of node voltages in nodes of the plurality of current paths (column 3, lines 4-46).

Regarding claim 22, Telewski and Thatcher et al. disclose the arrangement of claim 14 above. In addition, Thatcher et al. disclose wherein the test structure is further connected to the measurement unit (120), the test structure configured to access nodes of the at least one current path in order to measure the effective values of the node voltages (column 3, lines 35-46; figure 2).

Regarding claim 23, Telewski and Thatcher et al. disclose the arrangement of claim 14 above. In addition, Thatcher et al. disclose wherein the test structure is further connected to the current source (12), the test structure configured to access the network in order to supply current to the at least one current path (column 3, lines 35-46; figure 2).

5. Claims 11 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Telewski in view of Thatcher et al. and further in view of Walter et al. (US 4,611,101).

Regarding claims 11 and 24, Telewski and Thatcher et al. disclose the method and arrangement of claims 1 and 14 above, respectively. Telewski and Thatcher et al. do not specifically disclose the predefined network configuration includes a delta configuration. However, Walter et al. disclose a method and arrangement for testing

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communication device comprising several configurations including delta configuration (column 15, lines 44-49). Therefore, it would have been obvious to adapt the delta configuration of Walter et al to the method and arrangement of Telewski and Thatcher et al. in order to test the capacitance component of the electric circuit as suggest by Walter et al. (column 15, lines 44-49).

### ***Conclusion***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quochien B. Vuong whose telephone number is (571) 272-7902. The examiner can normally be reached on M-F 9:30-18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



**QUOCHIE B. VUONG**  
**PRIMARY EXAMINER**

Quochien B. Vuong  
June 25, 2006.